WE CLAIM:

1. A phase selector for generating a recovered clock signal, the phase selector comprising:

a phase select signal generator for generating a plurality of phase select signals in response to a FWD signal and a BWD signal from a digital filter;

wherein said digital filter asserts said FWD signal if the phase of a SDIN (serial digital input) signal leads the phase of said recovered clock signal;

and wherein said digital filter asserts said BWD signal if the phase of said SDIN (serial digital input) signal lags the phase of said recovered clock signal;

a multiplexer for inputting a predetermined number of given clock signals arranged in a predetermined phase order and for outputting a first output clock signal and a second output clock signal with said first and second output clock signals each being one of said given clock signals;

a phase interpolator that receives said first and second output clock signals from said multiplexer to generate said recovered clock signal having a phase that is phase interpolated between the phases of said first and second output clock signals; and

a multiplexer select control that controls said multiplexer to select one of said given clock signals for each of said first and second output clock signals, depending on whether said phase select signals indicate that said FWD signal is asserted or that said BWD signal is asserted such that the phase of said recovered clock signal generated from said phase interpolator increases when said FWD signal is asserted and decreases when said BWD signal is asserted and remains substantially constant when said FWD signal and said BWD signal are not asserted.

2. The phase selector of claim 1:

wherein said phase select signal generator is comprised of a plurality of bidirectional flip flops with each flip flop having an output signal that is a respective one

of said phase select signals;

and wherein said bidirectional flip flops are coupled together in a loop such that said phase select signals are arranged in a predetermined order with a selected one of said phase select signals being asserted as a currently asserted phase select signal with the rest of said phase select signals not being asserted;

and wherein a prior one from said currently asserted phase select signal in said order of said phase select signals is asserted as a newly asserted phase select signal when said BWD signal is asserted;

and wherein a subsequent one from said currently asserted phase select signal in said order of said phase select signals is asserted as said newly asserted phase select signal when said FWD signal is asserted;

and wherein a currently recovered clock signal is one of a chosen clock signal of said given clock signals, a leading interpolated clock signal of said chosen clock signal, or a lagging interpolated clock signal of said chosen clock signal,

and wherein said leading interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent leading clock signal in said predetermined phase order of said given clock signals;

and wherein said lagging interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent lagging clock signal in said predetermined phase order of said given clock signals;

and wherein when said currently recovered clock signal is said chosen clock signal, said multiplexer select control controls said multiplexer to select said chosen clock signal as said first output clock signal and to select said adjacent leading clock signal of said chosen clock signal as said second output clock signal, such that a newly recovered clock signal generated by said phase interpolator is said leading interpolated

clock signal of said chosen clock signal when said phase select signals indicate that said FWD signal is asserted;

and wherein when said currently recovered clock signal is said chosen clock signal, said multiplexer select control controls said multiplexer to select said chosen clock signal as said second output clock signal and to select said adjacent lagging clock signal of said chosen clock signal as said first output clock signal, such that said newly recovered clock signal generated by said phase interpolator is said lagging interpolated clock signal of said chosen clock signal when said phase select signals indicate that said BWD signal is asserted;

and wherein when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, said multiplexer select control controls said multiplexer to select, as said first and second output clock signals, an immediately leading one of said given clock signals having a phase that leads said currently recovered clock signal by a least phase amount, such that said newly recovered clock signal generated by said phase interpolator is said immediately leading one of said given clock signals when said phase select signals indicate that said FWD signal is asserted;

and wherein when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, said multiplexer select control controls said multiplexer to select, as said first and second output clock signals, an immediately lagging one of said given clock signals having a phase that lags said currently recovered clock signal by a least phase amount, such that said newly recovered clock signal generated by said phase interpolator is said immediately lagging one of said given clock signals when said phase select signals indicate that said BWD signal is asserted.

3. The phase selector of claim 2, wherein a first one of said loop of said bidirectional flip flops is a set flip flop, and wherein the rest of said bidirectional flip flops are reset flip flops, such that the phase select signal corresponding to said first one of said loop of

said bidirectional flip flops is asserted as said currently asserted phase select signal in response to a RST (reset) signal.

4. The phase selector of claim 3, wherein said loop of said bidirectional flip flops is a closed loop with said first one of said loop of said bidirectional flip flops being coupled to a last one of said loop of said bidirectional flip flops.

5. The phase selector of claim 1, wherein said predetermined number of given clock signals is sent to said multiplexer from a voltage controlled oscillator with any two adjacent given clock signals in said predetermined phase order of said given clock signals having a substantially same phase difference and with first and last given clock signals in said predetermined phase order of said given clock signals having said substantially same phase difference.

6. The phase selector of claim 1, further comprising:

another multiplexer for inputting said predetermined number of given clock signals and for outputting a third output clock signal that has a 180° phase shift from said first output clock signal and for outputting a fourth output clock signal that has a 180° phase shift from said second output clock signal; and

another phase interpolator that receives said third and fourth output clock signals to generate a complementary recovered clock signal that has a 180° phase shift from said recovered clock signal and that has a phase that is phase interpolated between the phases of said third and fourth output clock signals.

7. The phase selector of claim 1, wherein said phase selector comprises part of a DPLL (digital phase locked loop) within a SERDES (serializer/deserializer) transceiver.

8. A phase selector for generating a recovered clock signal, the phase selector comprising:

means for generating a plurality of phase select signals in response to a FWD signal and a BWD signal from a digital filter;

wherein said digital filter asserts said FWD signal if the phase of a SDIN (serial digital input) signal leads the phase of said recovered clock signal;

and wherein said digital filter asserts said BWD signal if the phase of said SDIN (serial digital input) signal lags the phase of said recovered clock signal;

and wherein said phase select signals are arranged in a predetermined order with a selected one of said phase select signals being asserted as a currently asserted phase select signal with the rest of said phase select signals not being asserted;

and wherein a prior one from said currently asserted phase select signal in said order of said phase select signals is asserted as a newly asserted phase select signal when said BWD signal is asserted;

and wherein a subsequent one from said currently asserted phase select signal in said order of said phase select signals is asserted as said newly asserted phase select signal when said FWD signal is asserted;

means for generating said recovered clock signal having a phase that is phase interpolated between a first phase of a first output clock signal and a second phase of a second output clock signal; and

means for selecting each of said first and second output clock signals as one of a predetermined number of given clock signals arranged in a predetermined phase order, depending on whether said phase select signals indicate that said FWD signal is asserted or that said BWD signal is asserted such that the phase of said recovered clock signal increases when said FWD signal is asserted and decreases when said BWD signal is asserted and remains substantially constant when said FWD signal and said BWD signal are not asserted.

9. The phase selector of claim 8:

wherein a currently recovered clock signal is one of a chosen clock signal of said given clock signals, a leading interpolated clock signal of said chosen clock signal, or a lagging interpolated clock signal of said chosen clock signal,

and wherein said leading interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent leading clock signal in said predetermined phase order of said given clock signals;

and wherein said lagging interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent lagging clock signal in said predetermined phase order of said given clock signals;

and wherein when said currently recovered clock signal is said chosen clock signal, said chosen clock signal is selected as said first output clock signal, and said adjacent leading clock signal of said chosen clock signal is selected as said second output clock signal, such that a newly recovered clock signal is said leading interpolated clock signal of said chosen clock signal when said phase select signals indicate that said FWD signal is asserted;

and wherein when said currently recovered clock signal is said chosen clock signal, said chosen clock signal is selected as said second output clock signal, and said adjacent lagging clock signal of said chosen clock signal is selected as said first output clock signal, such that said newly recovered clock signal is said lagging interpolated clock signal of said chosen clock signal when said phase select signals indicate that said BWD signal is asserted;

and wherein when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, an immediately leading one of said given clock signals having a phase that leads said currently recovered clock signal by a least phase

amount is selected as said first and second output clock signals, such that said newly recovered clock signal generated by said phase interpolator is said immediately leading one of said given clock signals when said phase select signals indicate that said FWD signal is asserted;

and wherein when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, an immediately lagging one of said given clock signals having a phase that lags said currently recovered clock signal by a least phase amount is selected as said first and second output clock signals, such that said newly recovered clock signal generated by said phase interpolator is said immediately lagging one of said given clock signals when said phase select signals indicate that said BWD signal is asserted.

10. The phase selector of claim 9, wherein a first one of said phase select signals is asserted as said currently asserted phase select signal in response to a RST (reset) signal.

11. The phase selector of claim 8, wherein said predetermined order of said phase select signals is a closed loop with a first phase select signal being adjacent a last phase select signal in said closed loop of said predetermined order of said phase select signals.

12. The phase selector of claim 8, wherein any two adjacent given clock signals in said predetermined phase order of said given clock signals have a substantially same phase difference, and wherein first and last given clock signals in said predetermined phase order of said given clock signals have said substantially same phase difference.

13. The phase selector of claim 8, further comprising:

means for generating a complementary recovered clock signal that has a 180° phase shift from said recovered clock signal and that has a phase that is phase

interpolated between the phases of third and fourth output clock signals, wherein said third output clock signal has a 180° phase shift from said first output clock signal, and wherein said fourth output clock signal has a 180° phase shift from said second output clock signal.

14. The phase selector of claim 8, wherein said phase selector comprises part of a DPLL (digital phase locked loop) within a SERDES (serializer/deserializer) transceiver.

15. A method for generating a recovered clock signal, comprising:

generating a plurality of phase select signals in response to a FWD signal and a BWD signal from a digital filter;

wherein said digital filter asserts said FWD signal if the phase of a SDIN (serial digital input) signal leads the phase of said recovered clock signal;

and wherein said digital filter asserts said BWD signal if the phase of said SDIN (serial digital input) signal lags the phase of said recovered clock signal;

and wherein said phase select signals are arranged in a predetermined order with a selected one of said phase select signals being asserted as a currently asserted phase select signal with the rest of said phase select signals not being asserted;

and wherein a prior one from said currently asserted phase select signal in said order of said phase select signals is asserted as a newly asserted phase select signal when said BWD signal is asserted;

and wherein a subsequent one from said currently asserted phase select signal in said order of said phase select signals is asserted as said newly asserted phase select signal when said FWD signal is asserted;

generating said recovered clock signal having a phase that is phase interpolated between a first phase of a first output clock signal and a second phase of a second output clock signal; and

selecting each of said first and second output clock signals as one of a predetermined number of given clock signals arranged in a predetermined phase order, depending on whether said phase select signals indicate that said FWD signal is asserted or that said BWD signal is asserted such that the phase of said recovered clock signal increases when said FWD signal is asserted and decreases when said BWD signal is asserted and remains substantially constant when said FWD signal and said BWD signal are not asserted.

16. The method of claim 15:

wherein a currently recovered clock signal is one of a chosen clock signal of said given clock signals, a leading interpolated clock signal of said chosen clock signal, or a lagging interpolated clock signal of said chosen clock signal,

and wherein said leading interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent leading clock signal in said predetermined phase order of said given clock signals;

and wherein said lagging interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent lagging clock signal in said predetermined phase order of said given clock signals;

the method of claim 15 further comprising:

selecting when said currently recovered clock signal is said chosen clock signal, said chosen clock signal as said first output clock signal, and said adjacent leading clock signal of said chosen clock signal as said second output clock signal, such that a newly recovered clock signal is said leading interpolated clock signal of said chosen clock signal when said phase select signals indicate that said FWD signal is asserted;

selecting when said currently recovered clock signal is said chosen clock signal,

said chosen clock signal as said second output clock signal, and said adjacent lagging clock signal of said chosen clock signal as said first output clock signal, such that said newly recovered clock signal is said lagging interpolated clock signal of said chosen clock signal when said phase select signals indicate that said BWD signal is asserted;

selecting when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, an immediately leading one of said given clock signals having a phase that leads said currently recovered clock signal by a least phase amount as said first and second output clock signals, such that said newly recovered clock signal is said immediately leading one of said given clock signals when said phase select signals indicate that said FWD signal is asserted; and

selecting when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, an immediately lagging one of said given clock signals having a phase that lags said currently recovered clock signal by a least phase amount as said first and second output clock signals, such that said newly recovered clock signal is said immediately lagging one of said given clock signals when said phase select signals indicate that said BWD signal is asserted.

17. The method of claim 16, wherein a first one of said phase select signals is asserted as said currently asserted phase select signal in response to a RST (reset) signal.

18. The method of claim 16, wherein said predetermined order of said phase select signals is a closed loop with a first phase select signal being adjacent a last phase select signal in said closed loop of said predetermined order of said phase select signals.

19. The method of claim 15, wherein any two adjacent given clock signals in said predetermined phase order of said given clock signals have a substantially same phase difference, and wherein first and last given clock signals in said predetermined phase order of

said given clock signals have said substantially same phase difference.

20. The method of claim 15, further comprising:

generating a complementary recovered clock signal that has a 180° phase shift from said recovered clock signal and that has a phase that is phase interpolated between the phases of third and fourth output clock signals, wherein said third output clock signal has a 180° phase shift from said first output clock signal, and wherein said fourth output clock signal has a 180° phase shift from said second output clock signal.

21. The method of claim 15, wherein said recovered clock signal is an output of a DPLL (digital phase locked loop) within a SERDES (serializer/deserializer) transceiver.

22. / A DPLL (digital phase locked loop) for generating a recovered clock signal, comprising:

a phase detector operable to compare a serial data input (SDIN) with a recovered clock signal (SCLK) and to generate in response up and down signals;

a digital filter coupled to the phase detector and operable to generate FWD (forward) and BWD (backward) signals in response to the up and down signals; and

a phase selector coupled to the digital filter and including a phase interpolator coupled to a multiplexer responsive to the FWD and BWD signals, the multiplexer operable to receive a plurality of given clock signals having different phases as inputs and to select each of at least two clock signals as one of the given clock signals as outputs, the phase interpolator operable to generate a recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals.

23. The DPLL (digital phase locked loop) of claim 22, wherein the DPLL (digital

phase locked loop) is part of a clock data recovery circuit within a SERDES (serializer/deserializer) transceiver.

24. The DPLL (digital phase locked loop) of claim 22, wherein the phase selector includes a phase select signal generator coupled to the multiplexor, the generator responsive to the FWD and BWD signals and operable to generate a multiplexer select signal.

25. The DPLL (digital phase locked loop) of claim 24, wherein the phase select generator comprises a plurality of bidirectional flip-flops with each flip-flop having an output signal that is a multiplexer select signal.

26. The DPLL (digital phase locked loop) of claim 22, wherein the multiplexer is operable to select the same clock signal as the at least two selected clock signals.

27. A phase selector comprising:

a phase select signal generator responsive to FWD (forward) and BWD (backward) signals and operable to generate a multiplexer select signal;

a multiplexer coupled to the phase select signal generator and operable to receive a plurality of given clock signals having different phases as inputs and to select each of at least two of the clock signals as one of the given clock signals as outputs; and

a phase interpolator coupled to the multiplexer and operable to generate a recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals.

28. A method for generating a recovered clock signal within a DPLL (digital phase locked loop) comprising:

comparing a serial data input (SDIN) with a recovered clock signal (SCLK) and

generating in response up and down signals;

generating FWD (forward) and BWD (backward) signals in response to the up and down signals;

selecting at least two clock signals from a plurality of given clock signals having different phases in response to the FWD and BWD signals; and

generating the recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals.

29. A method for generating a recovered clock signal comprising:

providing a plurality of given clock signals having different phases;

selecting each of at least two clock signals as one of the given clock signals in response to received FWD (forward) and BWD (backward) signals; and

generating a recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals.

30. The method of claim 29, wherein said step of selecting at least two clock signals includes the step of selecting the same clock signal as the at least two clock signals.